This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-21. (Canceled).

22. (Withdrawn) A method of making a semiconductor package comprising the steps of:

a) punching vias in at least two low temperature co-fired ceramic layers;

b) filling the vias with a conductor;

c) screen printing conductor lines on the layers;

d) screen printing a seal ring and a plurality of pads on one of the layers;

e) screen printing a plurality of ball pads on one of the layers;

f) stacking the layers;

g) laminating under pressure the layers into a substrate;

h) firing the substrate in an oven;

i) depositing a rigid support on the substrate;

j) screening a first solder paste onto the seal ring and the pads;

k) placing a micro-machined semiconductor device onto the substrate;

l) reflowing the first solder paste in an oven such that the micro-machined semiconductor device is attached to the substrate;

m) screening a second solder paste onto the ball pads;

n) placing a plurality of solder spheres onto the ball pads; and

o) reflowing the second solder paste in an oven such that the solder spheres are attached to the ball pads.

23. (Withdrawn) The method according to claim 22, wherein the rigid support is an ultrasonically deposited metal.

24. (Withdrawn) The method according to claim 22, wherein the metal is chosen from the group consisting of:

a) gold; and

b) an alloy of gold and palladium.

25. (Currently amended) A semiconductor package comprising:

a planar low temperature co-fired ceramic substrate having a first and second layer mounted adjacent each other, the first layer having a first surface and the second layer having a second surface,

a micro-machined semiconductor device located adjacent the first surface, the micro-machined semiconductor device having a plurality of first pads and an active central area;

a plurality of ball pads located on the second surface;

a plurality of second pads located on the first surface;

a plurality of vias, extending through the substrate between the first and second surfaces, the vias connected to the ball pads and to the first pads;

a reflowed solder joint located between the first and second pads for electrically connecting the substrate to the semiconductor device, the reflowed solder joint formed from a first reflowed solder paste;

a solder seal ring, located between the micro-machined semiconductor device and the first surface around an outer perimeter of the substrate for making a hermetic seal between the micro-machined semiconductor device and the substrate;

a plurality of ultrasonically deposited wire bond bumps located between the micro-machined semiconductor device and the first surface for supporting the micro-machined semiconductor device during assembly and preventing the micro-machined semiconductor device from contacting the first surface during reflow of the solder joint, the wire bond bumps further spacing the micro-machined semiconductor device from the first surface, the wire bond bumps further arranged around the active area, the wire bond bumps formed from a metal; ~~and~~

a plurality of solder spheres mounted to the ball pads by a second reflowed solder paste; and

wherein the substrate does not have a cavity.

26. (Previously presented) The semiconductor package according to claim 25, wherein a plurality of circuit lines are located on the first surface, the circuit lines connected between the vias and the second pads.

27. (Canceled).

28. (Previously presented) The semiconductor package according to claim 25, wherein the wire bond bumps are formed from either gold or an alloy of gold.